AMENDMENTS TO THE SPECIFICATION

Please substitute the following replacement paragraphs for like-numbered paragraphs of the specification:

[0031] In one embodiment, each of the even compare line pairs 358/360 is coupled to an even comparand register 310 and used to conduct a pair of complementary compare signals representative of a respective constituent bit of an even comparand value (i.e., stored in the register 310) to the corresponding column of CAM cells 351. Similarly, each of the odd compare line pairs 362/364 is coupled to an odd comparand register 308 and used to conduct a pair of complementary compare signals representative of a respective constituent bit of an odd comparand value (i.e., stored in the register 308) to the corresponding column of CAM cells 351.

In an alternative embodiment, single-ended compare signals may be delivered to the columns of the CAM cells such that two compare lines may be used to form a given compare line group 361, rather than the four compare lines per group shown in Figure 5. Also, in a pipelined system, a single comparand register may be used to drive signals onto the even and odd compare line pairs at different times. In yet other embodiments, the comparand registers may be omitted altogether, with the even and odd compare line pairs being driven directly (and either simultaneously or in time-multiplexed fashion) by comparand data signals received via an external interface. Note that, while the compare signals present on a compare line pair are generally referred to herein as being complementary comparand signals, both compare lines of a compare line pair may be driven to the same state (low or high), for example, to mask compare operations within an entire column of the CAM array 350.

[0037] Still referring to Figure 6, compare circuit 385 includes a pair of compare sub-circuits 387/389 coupled in parallel with one another between reference node 412 (a ground node in this example, though other reference voltages may be used) and match line 384 (ML1), and compare circuit 395 similarly includes a pair of compare sub-circuits 397/399 coupled in parallel with one another between reference voltage node 414 and match line 386 (ML2). Referring specifically to compare circuit 385, sub-circuit 387 includes transistors 401 and 403 coupled in series between match line 384 and reference node 412, and sub-circuit 389 includes transistors 405 and 407 also coupled in series between match line 384 and reference node 412. In compare circuit 395, sub-circuit 397 includes transistors 411 and 413 coupled in series between match line 386 and reference node 414, and sub-circuit 399 includes transistors 415 and 417 also coupled in series

between match line 386 and the reference node 414. Control terminals of transistors 403 and 413 (i.e., MOS transistor gates in this example) are coupled to X-cell 381 and therefore are switched on or off according to the state of the X-bit of a quaternary data value, and control terminals of transistors 407 and 417 are coupled to Y-cell 383 and are therefore switched on or off according to the state of the Y-bit of the quaternary data value. Transistors 405 and 401 are coupled to compare lines 396 and 398, respectively and are therefore switched on or off according to the state of comparand signals C1 and /C1 presented on the compare line pair 396/398. Transistors 415 and 411 are similarly coupled to compare lines 400 and 402, respectively, and are therefore switched on or off according to the state of comparand signals C2 and /C2 presented on the compare line pair 400/402. Thus, match line 384 is switchably coupled to reference node 412 via transistor pair 401/403 of compare sub-circuit circuit 387, and via transistor pair 405/407 of compare sub-circuit 389. Similarly, match line 386 is switchably coupled to reference node 414 via transistor pair 411/413 of compare sub-circuit 399 and via transistor pair 415/417 of compare sub-circuit 399.

[0050] Figure 12 illustrates a circuit arrangement for reading and writing data in an array 302 of multi-compare quaternary CAM cells. An address decoder 338 activates one of a plurality of word lines indicated by an address value (ADDR) to enable read and write access to a selected row of CAM cells within the array 302 (i.e., the row of CAM cells selected by the address value). In a read operation, read circuitry within a read/write circuit 501 senses a data word output onto bit lines 502 from the selected row of CAM cells and outputs the data word, referred to herein as read data word, onto a data bus 508. The data bus 508 may be ~~a~~ dedicated to providing read and write access to the CAM array 302, or may be time multiplexed with comparand data, result data and/or instruction data (e.g., the data bus 508 may be the CBUS 318, RBUS 328 or IBUS 320 of Figure 3). In a write operation, a write data word is received via the data bus 508 and input to a data word translator 503. In one embodiment, the data word translator 503 generates a translated data word (also referred to herein as an encoded data word) based on data and mask bits within the incoming write data word, then selects, according to the state of a data select signal 506 (DSEL), either the translated data word or the write data word to be output to the read/write circuit 501 via write data path 510. Write driver circuits within the read/write circuit 501 drives the selected data word (i.e., the data word output from the data word translator 503) onto the bit lines 502 of the CAM array 302 for storage in an address-selected row of CAM cells. In an alternative embodiment, the data word translator 503 additionally

receives a read data word from the read/write circuit 501 (e.g., via path 508) to enable a data word read from a source row of CAM cells within the CAM array 302 to be transferred to a destination row of CAM cells. In a first type of transfer operation, referred to herein as a copy operation, the content of the source row (i.e., the row of CAM cells which from which a read data word is read) is unaffected by the storage of the read data word in the destination row. In a second type of transfer operation, referred to herein as a move operation, the content of the source row is invalidated (e.g., by flipping one or more bits indicative of row validity, or by storing a predetermined value within the row) as part of the transfer operation. The source row may be invalidated during the data read operation (e.g., by driving bit lines coupled to a column of validity CAM cells to store an invalid state for the source row); after the data read operation, but prior to or during data word storage in the destination row; or after the data word is stored in the destination row. In another alternative embodiment, the data word translator 503 and data word selector may be omitted altogether, with any desired data word translation being performed by the write requestor or other external circuitry.

[0070] In an alternative embodiment, an additional expansion circuit 651 may be provided per pair of CAM cell rows and used to generate a second composite match signal based on the state of the match lines 322, 324 that are not coupled to the existing expansion circuit. For example, an additional expansion circuit 651 may be coupled to odd match line 324_1 and even match line 322_2 to generate a composite match signal according to the states of component match signals on those match lines. The word-length select signal 675 or a separate select signal may be supplied to a select circuit (not shown) to select either the composite match signal or the component match signal on odd match line 324_1 to be output to the priority encoding circuit 673. Alternatively, the word-length select signal 675 (or separate select signal) may be input to a select circuit to select either the composite match signal or the component match signal on even match line 322_2 to be output to the priority encoding circuit 672. Also, the component match signal on match line 324_2 may be sent to one or both of the priority encoding circuits 672, 673 in addition to the component match signals on match lines 322_1, 322_2, 324_1 and the composite match signal 668.

[0075] One application of the match circuitry 685 is to enable storage of double-word data values starting at either odd or even CAM row boundaries. That is, in contrast to the embodiment of Figure 16 in which double-word data values are stored on odd-row boundaries (i.e., double-word data value spans from an odd-numbered CAM row to a higher, even-

numbered CAM row (e.g., 1 to 2, 3 to 4, etc.)), double-word data values may additionally be stored on even-row boundaries (e.g., 2 to 3, 4 to 5, etc.). When the word-length select signal 675 selects a double-word compare mode, the composite match signals resulting from matches with double-word data values stored on odd-row boundaries (i.e., odd-bound composite match signals $668_{1,2}$, $668_{3,4}$, etc.) are output to an odd priority encoding circuit 673 within the priority encoder 679, and the composite match signals resulting from matches with double-word data values stored on even-row boundaries (i.e., even-bound composite match signals $668_{2,3}$, $668_{4,5}$, etc.) are supplied to an even priority encoding circuit 672 within the priority encoder 679. In the embodiment of Figure 17, a double-word boundary signal 677 (DWB) is supplied to the even and odd priority encoding circuits 672 and 673 to disable one priority encoding circuit or the other according to a selected double-word boundary. For example, if an odd double-word boundary is selected (e.g., by instruction, programmed mode, etc.) and a double-word compare mode is enabled, the double-word boundary signal 677 is set to a first state to enable match address encoding within the odd priority encoding circuit 673 and to disable match address encoding within the even priority encoding circuit 672. This may be accomplished, for example, by selectively disabling match indications at an input to the encoding logic within circuits 672 and 673 (e.g., by ANDing even-bound composite match signals with the double-word boundary select signal and ANDing odd-bound composite match signals with a complement of the double-word boundary select signal), selectively disabling an output of the priority encoding circuits 672 and 673, or disabling other logic functions within the priority encoding circuits 672 and 673. It should be noted that the CAM row numbering in Figure 17 may alternately start at zero and extend to N-1, in which case the semantic of odd and even double-word boundaries may be reversed.

[0092] The first stage composite match signals 775_1-775_N are provided in respective pairs to logic AND gates 777_1-$777_{N/4}$ (only the first two of which are shown in Figure 22) within logic circuit 776 which, in turn, generates second stage composite match signals 779_1-$779_{N/4}$. For example, first stage composite match signals 775_1 and 775_2 are input to AND gate 777_1 to generate second stage composite match signal 779_1; first stage composite match signals 775_3 and 775_4 are input to AND gate 777_2 to generate second stage composite match signal 779_2; and so forth. The second stage composite match signals 779 are provided to respective third inputs (i.e., '2' inputs) of component multiplexers 781_1-781_N. Because there are one-fourth as many second stage composite match signals 779 as first stage match signals 771, only one-fourth of the

component multiplexers 781 (i.e., every fourth one) are coupled to receive second stage composite match signals 779, with the connections made on boundaries of lowest numbered CAM rows. Component multiplexers 781 not coupled to receive a second stage composite match signal ~~775~~ 779 are grounded at the third input, or otherwise configured to prevent match indication. For example, composite match signals 779_1, 779_2, ..., $779_{N/4}$ are provided to the third inputs of component multiplexers 781_1, 781_5, ..., 781_{N-3}, while the third inputs of component multiplexers 781_2-781_4, 781_6-781_8,..., 781_{N-2}-781_N are grounded.

[0093] Each of the component multiplexers 781 includes a select input (not shown in Figure 22) coupled to receive a word-select signal 782. The word-select signal 782 is a multi-bit signal having at least as many bits as necessary to enable selection of the different stages of match signals to be output from the multiplexer 780 to the priority encoder 306 as final match signals 783_1-783_N. In one embodiment, for example, the word-select signal 782 is an encoded, two-bit signal in which states '00', '01' and '10' are used to select the first stage match signals 771_1-771_N, first stage ~~component~~ composite match signals 775_1-$775_{N/2}$, and second stage ~~component~~ composite match signals 779_1-$779_{N/4}$, respectively, to be output to the priority encoder 306. Thus, when the word-select signal 782 is set to the '00' state, first stage match signals 771_1-771_N are output as final match signals 783_1-783_N to corresponding priority encoder inputs PE1-PE(N). When the word-select signal 782 is set to the '01' state, first stage ~~component~~ composite match signals 775_1-$775_{N/2}$ are output as final match signals 783_1, 783_3, 783_5..., 783_{N-1} to corresponding priority encoder inputs PE1, PE3, PE5, ..., PE(N-1), and the unused final match signals 783_2, 783_4, 783_6, ..., 783_N are forced to a non-match state (e.g., grounded). Similarly, when the word-select signal 782 is set to the '10' state, second stage ~~component~~ composite match signals 779_1-$779_{N/4}$ are output as final match signals 783_1, 783_5, ..., 783_{N-3} to corresponding priority encoder inputs PE1, PE5, ..., PE(N-3), and the unused final match signals 783_2-783_4, 783_6-783_8, ..., 783_{N-2}-783_N are forced to a non-match state. In an alternative embodiment, different encodings of the word-select signal 782 may be used to select the different stages of match signals. Also, rather than being encoded, the word-select signal 782 may include as many constituent bits as match signal stages, with a given bit being active (i.e., high or low) at a time to select the corresponding stage of match signals.